

Instruction	Size	Address modes for [ea]									Flags				
		#	dn	an	(an)	(an)+	-(an)	$\pm K_{16}(an)$	$\pm K_8(an, Ri)$	Abs	X	N	Z	V	C
add [ea],dx	BWL	*	*	*	*	*	*	*	*	*	✓	✓	✓	✓	✓
add dx,[ea]	BWL				*	*	*	*	*	*	✓	✓	✓	✓	✓
adda [ea],ax	WL	*	*	*	*	*	*	*	*	*	•	•	•	•	•
addi #K,[ea]	BWL		*	*	*	*	*	*	*	*	✓	✓	✓	✓	✓
addq #K <sub>3</sub> ,[ea]	BWL		*	*	*	*	*	*	*	*	✓	✓	✓	✓	✓
and [ea],dx	BWL	*	*		*	*	*	*	*	*	•	✓	✓	0	0
and dx,[ea]	BWL				*	*	*	*	*	*	•	✓	✓	0	0
andi #K,[ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	0	0
asl/r dx,dy	BWL										✓	✓	✓	✓	✓
asl/r K <sub>3</sub> ,dx	BWL										✓	✓	✓	✓	✓
asl/r [ea]	W				*	*	*	*	*	*	✓	✓	✓	✓	✓
bccf [label]	BW	See table on Page 2									•	•	•	•	•
bra [label]	BW										•	•	•	•	•
bsr [label]	BW										•	•	•	•	•
btst #K,dx	L										•	•	✓	•	•
btst #K,[ea]	B				*	*	*	*	*	*	•	•	✓	•	•
clr [ea]	BWL		*		*	*	*	*	*	*	•	0	1	0	0
cmp [ea],dx	BWL	*	*	*	*	*	*	*	*	*	•	✓	✓	✓	✓
cmpa [ea],ax	WL	*	*	*	*	*	*	*	*	*	•	✓	✓	✓	✓
cmpi #K,[ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	✓	✓
divs [ea],dx	W	*	*		*	*	*	*	*	*	•	✓	✓	✓	0
divu [ea],dx	W	*	*		*	*	*	*	*	*	•	✓	✓	✓	0
eor dx,[ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	0	0
eori #K,[ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	0	0
exg Rx,Ry	L										•	•	•	•	•
ext dx	WL										•	✓	✓	0	0
jmp [ea]					*			*	*	*	•	•	•	•	•
jsr [ea]					*			*	*	*	•	•	•	•	•
lsl/r dx,dy	BWL										✓	✓	✓	0	✓
lsl/r K <sub>3</sub> ,dx	BWL										✓	✓	✓	0	✓
lsl/r [ea]	W				*	*	*	*	*	*	✓	✓	✓	0	✓
move [ea],[ea]	BWL	* <sup>S</sup>	*	* <sup>S</sup>	*	*	*	*	*	*	•	✓	✓	0	0
move [ea],ccr	W	*	*		*	*	*	*	*	*	✓	✓	✓	✓	✓
move [ea],sr <sup>P</sup>	W	*	*		*	*	*	*	*	*	✓	✓	✓	✓	✓
movea [ea],ax	WL	*	*	*	*	*	*	*	*	*	•	•	•	•	•
movem [ΣR <sub>m</sub> ],[ea]	WL				*		*	*	*	*	•	•	•	•	•
movem [ea],[ΣR <sub>m</sub> ]	WL				*	*	*	*	*	*	•	•	•	•	•
moveq #±K <sub>8</sub> ,dx	L										•	✓	✓	0	0
mulu [ea],dx	W	*	*		*	*	*	*	*	*	•	✓	✓	0	0
neg [ea]	BWL		*		*	*	*	*	*	*	✓	✓	✓	✓	✓
nop											•	•	•	•	•
not [ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	0	0

✓ : Flag operates in the normal manner. • : Not affected. P : Privileged.  
 a<sub>n</sub> : Address register n. S : Source only. \* : Available.  
 d<sub>n</sub> : Data register n. K<sub>m</sub> : m-bit constant. ± : Signed.  
 R<sub>n</sub> : Data or Address register n. ccf : Code Condition Flags. ccr : Code Condition Register.  
 sr : Status register. ΣR<sub>m</sub> : Any collection of Data/Address registers.  
 B : Byte size. W : Word size. L : Long-word size.

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or [ea],dx	BWL	*	*		*	*	*	*	*	*	•	✓	✓	0	0
or dx,[ea]	BWL				*	*	*	*	*	*	•	*	✓	0	0
ori #K,[ea]	BWL		*		*	*	*	*	*	*	•	*	✓	0	0
ori #K,sr <sup>P</sup>	W										✓	✓	✓	✓	✓
rol/r dx,dy	BWL										•	✓	✓	0	✓
rol/r K <sub>3</sub> ,dx	BWL										•	✓	✓	0	✓
rol/r [ea]	W				*	*	*	*	*	*	•	✓	✓	0	✓
roxl/r dx,dy	BWL										✓	✓	✓	0	✓
roxl/r K <sub>3</sub> ,dx	BWL										✓	✓	✓	0	✓
roxl/r [ea]	W				*	*	*	*	*	*	✓	✓	✓	0	✓
rte <sup>P</sup>											✓	✓	✓	✓	✓
rts											•	•	•	•	•
sub [ea],dx	BWL	*	*	*	*	*	*	*	*	*	✓	✓	✓	✓	✓
sub dx,[ea]	BWL				*	*	*	*	*	*	✓	✓	✓	✓	✓
suba [ea],ax	WL	*	*	*	*	*	*	*	*	*	•	•	•	•	•
subi #K,[ea]	BWL		*		*	*	*	*	*	*	✓	✓	✓	✓	✓
subq K <sub>3</sub> ,[ea]	BWL		*	*	*	*	*	*	*	*	•	✓	✓	✓	✓
swap dx	W										•	✓	✓	0	0
trap #K <sub>4</sub>											•	•	•	•	•
tst [ea]	BWL		*		*	*	*	*	*	*	•	✓	✓	0	0

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 R<sub>n</sub> : Data or Address register n. ccf : Code Condition Flags. ccr : Code Condition Register.  
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Conditional Branches, Bccf					
beq	Equal	Z=1	bvc	oVerflow Clear	V=0
bne	Not Equal	Z=0	bvs	oVerflow Set	V=1
bcc	Carry Clear	C=0	bp <sub>l</sub>	PLus	N=0
bcs	Carry Set	C=1	bmi	MInus	N=1
bhs	Higher or Same	C=0	bge	Greater or Equal	N⊕V=0
bhi	Higher than	C+Z=0	blt	Less Than	N⊕V=1
bls	Lower or Same	C+Z=1	bgt	Greater Than	$\overline{N\oplus V} \cdot \overline{Z} = 1$
blc	LOwer than	C=1	b <sub>l</sub> e	Less or Equal	$\overline{N\oplus V} \cdot \overline{Z} = 0$